Rock Solid Rf

Get pinpoint precision with this PLL-based frequency synthesizer.

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The main problem radio amateurs face in constructing a receiver or transceiver is ensuring constant frequency of the receiver heterodyne or the transmitter frequency. It is not so difficult to ensure stable operation of a vfo operating on a relatively low frequency and within a fixed range. The problem lies in ensuring constant frequency of an oscillator which has to operate within various bands (10, according to the latest band plan) and on a relatively high frequency.

The problem may be solved by using switched crystal oscillators in the band generator or by using the PLL (phase-locked loop) method when constructing the band oscillator. The use of this method under nonprofessional conditions is difficult since the system is quite complex and involves the use of proper programmed dividers and a filter in the vco control system which is difficult to optimize and which has to operate over a large frequency range.

My solution is to use the FLL (frequency-locked loop) method for frequency stabilization of the band oscillator. The advantages of this method are a relatively simple system and the possibility of applying it to already-constructed equipment. The use of the FLL

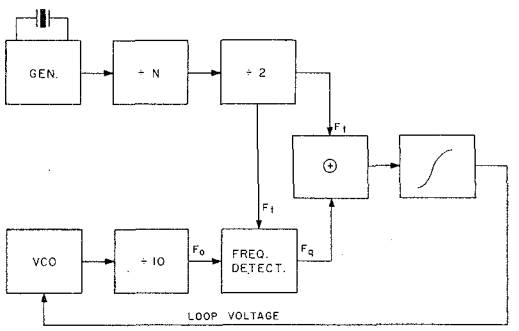

Fig. 1. Principle of operation of FLL synthesizer.

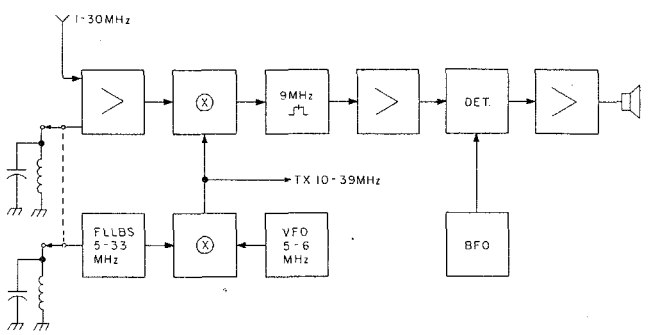

Fig. 2. Block diagram of radio receiver.

Received frequency F_R (MHz)	FLLBS frequency F_{H1} (MHz)	Vfo frequency F_{H2} (MHz)	Output frequency of heterodyne mixer (MHz)
1- 2	5.0		10-11
3- 4	7.0		12-13
7- 8	11.0		16-17
10-11	14.0		19-20
14-15	18.0	5-6	23-24
18-19	22.0		27-28
21-22	25.0		30-31
24-25	28.0		33-34
28-29	32.0		37-38
29-30	33.0		38-39

Table 1.

method for frequency stabilization of LC generators in the already-constructed equipment involves minimum system alterations while it considerably improves frequency stability.

Fig. 1 explains the principle of operation of the FLL system. The essential part is a flip-flop, type D, which functions as a harmonic mixer. Signals F_o from the vco and the clock signal, F_t, obtained from the quartz generator are supplied to its inputs D and C. The output signal of the flip-flop element, F_q, is expressed by the formula: $F_q = F_o - kF_t$, where k is a positive integer.

Obtaining the values of F_t and F_q as constants, we can change the frequency F_o in a function of the harmonic number k. In order to ensure constant frequency F_q, this frequency was compared with frequency F_t from the quartz generator. Both signals, F_t and F_q, are transformed into impulses with opposite polarization; added, their mean value is formed in the integrator, and they are amplified. From the amplifier output, the voltage of error is taken to adjust the frequency of the vco. Frequency F_q was, in my case, set at 50 Hz. Since frequencies F_t and F_q differ substantially, voltage levels F_t and F_q when added were also differentiated.

The Radio Receiver

The synthesizer constructed by me with the help of the FLL method is thought to be part of a radio receiver (and a transceiver in the future). A block diagram is shown in Fig. 2. As can be seen, the receiver system is of a conventional type. Single-frequency conversion was used with an i-f of 9 MHz. The vfo operates in the frequency range of 5 to 6 MHz. The receiver has ten bands. The determination of basic frequencies according to the formula $F_R = (F_{H1} + F_{H2}) - F_{i\text{-}f}$ and the determinations of the FLLBS synthesizer frequencies are given in Table 1.

The vfo is of a conventional construction: It is an LC generator. I intend to build a vfo also based on the FLL method, however. When constructing the whole receiver or transceiver, it is also possible to use the microprocessor vfos described in *73* (June, 1982); that output frequency is also 5-6 MHz.

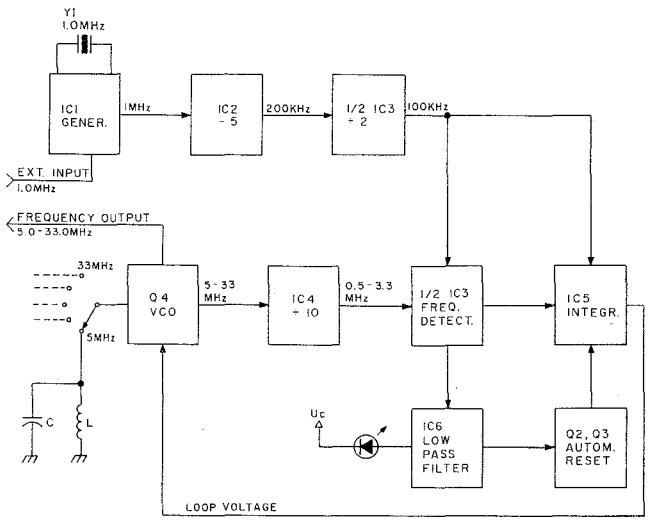

Fig. 3. Block diagram of band synthesizer.

The FLLBS Synthesizer

A block diagram of the synthesizer is presented in Fig. 3, while its schematic diagram is shown in Fig. 4 (digital part) and Fig. 5 (the vco). As can be seen from the drawings, the synthesizer is of a simple construction: All that is needed are several standard elements, and the cost of this system should not exceed ten to fifteen dollars.

The operation of individual parts of the system is as follows:

- The 1.0-MHz crystal oscillator is a typical one; it can operate on its own crystal or from an external 1.0-MHz generator.
- The next element (IC2) operates as a divider by 5; at its output (pin 11), a frequency of 200 kHz is obtained.
- The frequency detector (IC3) is based on a 7474 flip-flop. At its clock input (pin 11, IC3), a frequency of 100 kHz is supplied, obtained by dividing 200 kHz by the first flip-flop of IC3. To the input D of the detector (pin 12, IC3), a frequency obtained from the vco, preliminarily divided by 10 in the IC4 counter, is supplied.

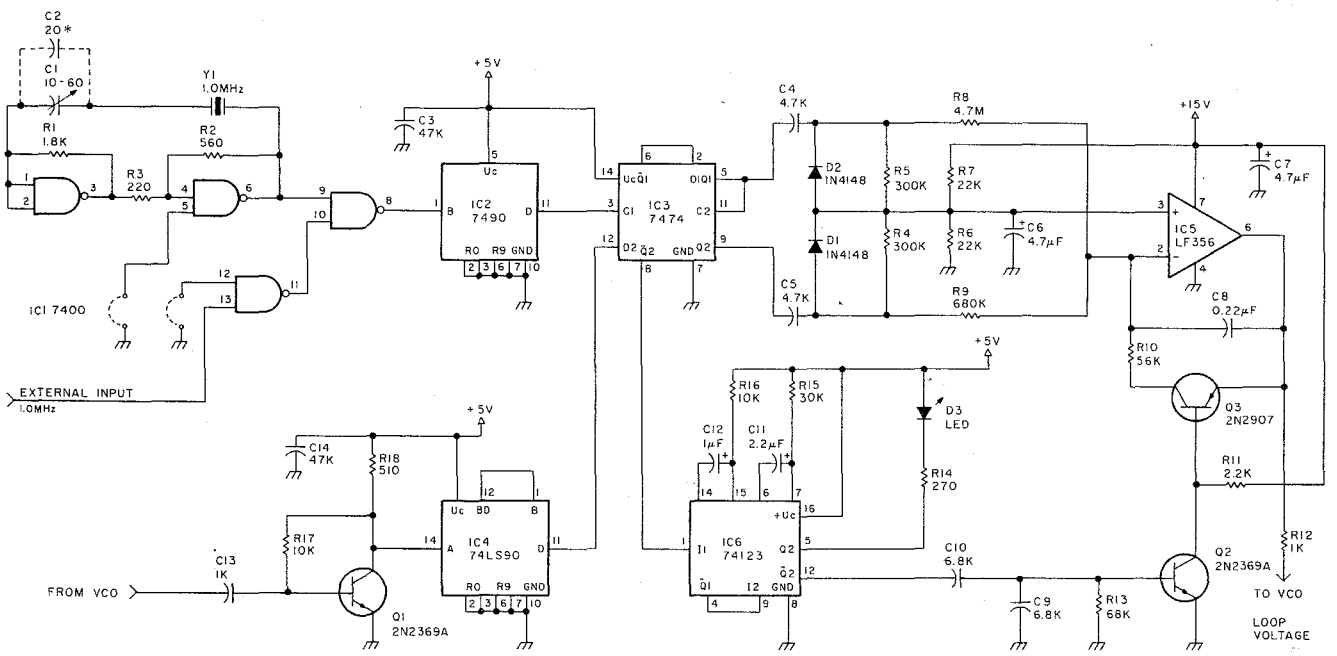

Fig. 4. Digital part of band synthesizer (FLLBS).

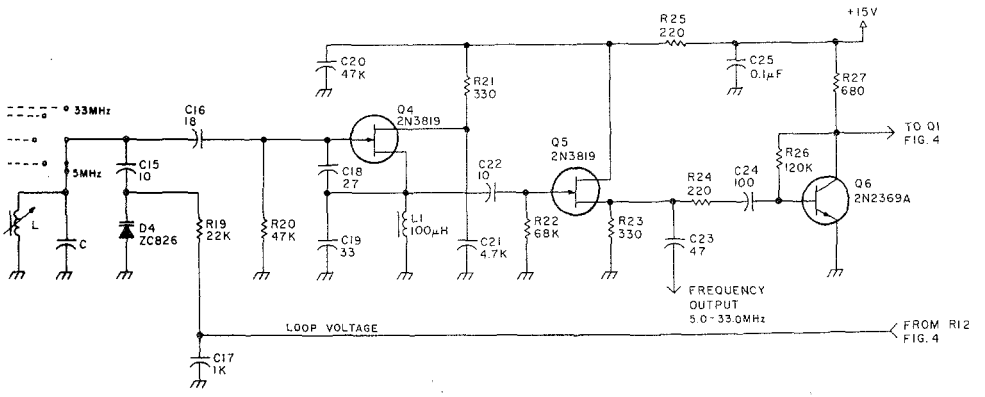

Fig. 5. Vco of band synthesizer.

- IC5 operates as an integrator; due to high resistances in the adding circuit, I constructed it with the use of an FET amplifier with high input resistance.
- IC6 functions as a low-pass filter; it has to detect and signal through the diode LED the state of desynchronization of the frequency-locked loop. Transistors Q2 and Q3 serve to neutralize the integrator when the vco is desynchronized and restore the state of synchronization of the loop.
- Desynchronization often takes place when changing the bands of the vco.
- The vco (Fig. 5) operates in a standard system. For individual operating bands (see Table 1), separate resonance circuits were used, changed by selector switch together with the corresponding input circuits of the receiver. The function of the switch may be also performed by contacts of relays. For tuning the vco, a varicap diode was used. At the generator output, a voltage follower from which the output signal is taken was used. The signal from the follower is amplified by transistors Q6 and Q1 and supplied to the counter from IC4.

Construction and Alignment of the FLLBS

The digital part of the system and the vco were placed on separate printed circuit boards. The purpose of this was to eliminate disturbing pulses from the digital part which could reach the receiver input through the vco. Depending on the actual mechanical design of the receiver, it might be necessary to enclose the digital part of the synthesizer in a shielded casing.

The vco, the voltage follower, and one stage of the amplifier were placed on a plate with the resonance circuits and the band-selector switch. Figs. 6 and 7 show the digital part of the synthesizer. The construction of the vco depends on the type of the band-selector switch used and the coil casing of the resonance circuits. The design of the vco PC board should be worked out individually, depending on the needs.

For the same reasons, I am not giving here the data for the LC circuits for individual bands; they should be selected according to the generally-known principles. All transistors and diodes used in my construction may be replaced by their more recent equivalents.

When aligning the crystal oscillator, pins 5 and 12 of IC1 should be properly connected. When working with a built-in crystal, pin 12 should be connected to ground and pin 5 left free; when using an external oscillator, it should be connected to the proper terminal pins of the PC board and pin 5 should be connected to ground, while pin 12 should be left free.

When aligning the synthesizer, a voltmeter should be connected to output 6 of IC5 and then controlling the vco frequency meter or a calibrated receiver, the vco resonance circuit of the vco should be tuned by means of the coil core to a fre-

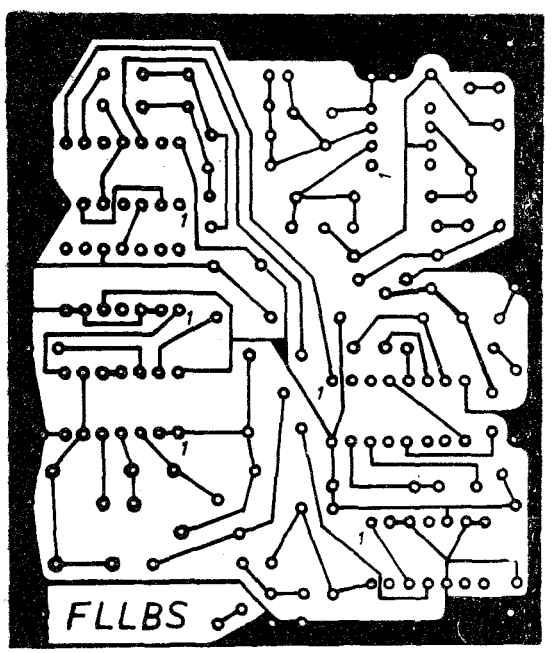

Fig. 6. Digital part of FLLBS PC board (foil side).

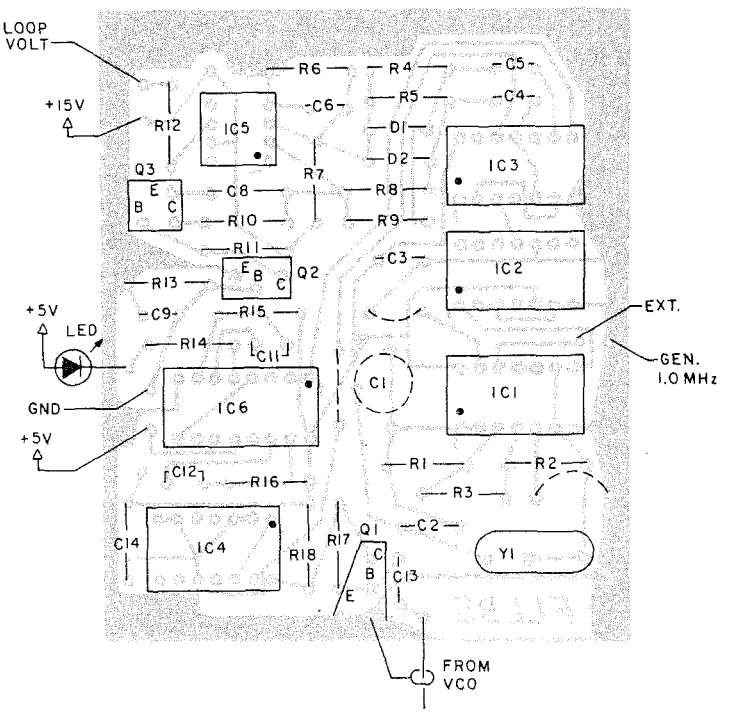

Fig. 7. FLLBS, component placement.

quency close to the required frequency until the vco is synchronized. When synchronizing the oscillator, the LED should go out.

To obtain a maximum range of loop synchronization, the vco resonance circuit should be tuned in such a way that the voltmeter shows about 11 V. The above method of aligning should be repeated for all operating bands of the synthesizer.

Other Applications of FLLBS

The FLL band synthesizer described above operates with an interval equal to 1 MHz. In case it is used for oscillator stabilization with a different frequency interval, the frequency F_t should be selected accordingly. For instance, in a generator operating with an interval equal to 500 kHz, the frequency F_t should be reduced at output 3 of IC3 from 200 kHz to 100 kHz (IC2 should be changed so that it could divide by ten). No other change is needed.

When the FLLBS is used for oscillator stabilization in the already-constructed equipment, besides choosing the correct frequency, F_t, a varicap diode should be built into the existing oscillator through the correct padding capacity and the resonance circuits should be tuned into the loop synchronization range. The loop synchronization range depends on changes in the capacity of the varicap diode and the value of the padding capacitor, C15.

A capacitor with a relatively low capacity was used here to make impossible any accidental synchronization of the vco with the frequency different by ±1 MHz from the desired frequency. The operation of the vco and its synchronization were tested up to about 60 MHz; synchronization was correct within the whole range. If we want to use the FLLBS for operation at higher frequencies than 60 MHz, IC4 should be replaced with a fast-series IC. Capacitor C15 should be reduced and the vco resonance circuits should be selected and tuned; no other changes are necessary. ■

Parts list

Component	Value	Quantity	Component	Value	Quantity
R1	1.8k	1	C4, 5, 21	4.7k	3
R2	560	1	C6, 7	4.7 uF	2
R3, 24, 25	220	3	C8	0.22 uF	1
R4, 5	300k	2	C9, 10	6.8k	2
R6, 7, 19	22k	3	C11	2.2 uF	1
R8	4.7 Meg	1	C12	1 uF	1
R9	680k	1	C13, 17	1k	2
R10	56k	1	C15, 22	10 pF	2
R11	2.2k	1	C16	18 pF	1
R12	1k	1	C18	27 pF	1
R13, 22	68k	2	C19	33 pF	1
R14	270	1	C23	47 pF	1
R15	30k	1	C24	100 pF	1
R16, 17	10k	2	C25	0.1 uF	1
R18	510	1	Q1, 2, 6	2N2369A	3
R20	47k	1	Q3	2N2907	1
R21, 23	330	2	Q4, 5	2N3819	2
R26	120k	1	D1, 2	1N4148	2
R27	680	1	D4	ZC826	1
L1	100 uH	1	D3	LED	1
Y1	1.0 MHz	1	IC1	SN7400	1
C1	10–60 pF var.	1	IC2	SN7490	1
			IC3	SN7474	1
C2	20 pF if needed	1	IC4	SN74LS90	1
			IC5	LF356	1
C3, 14, 20	47k	3	IC6	SN74123	1