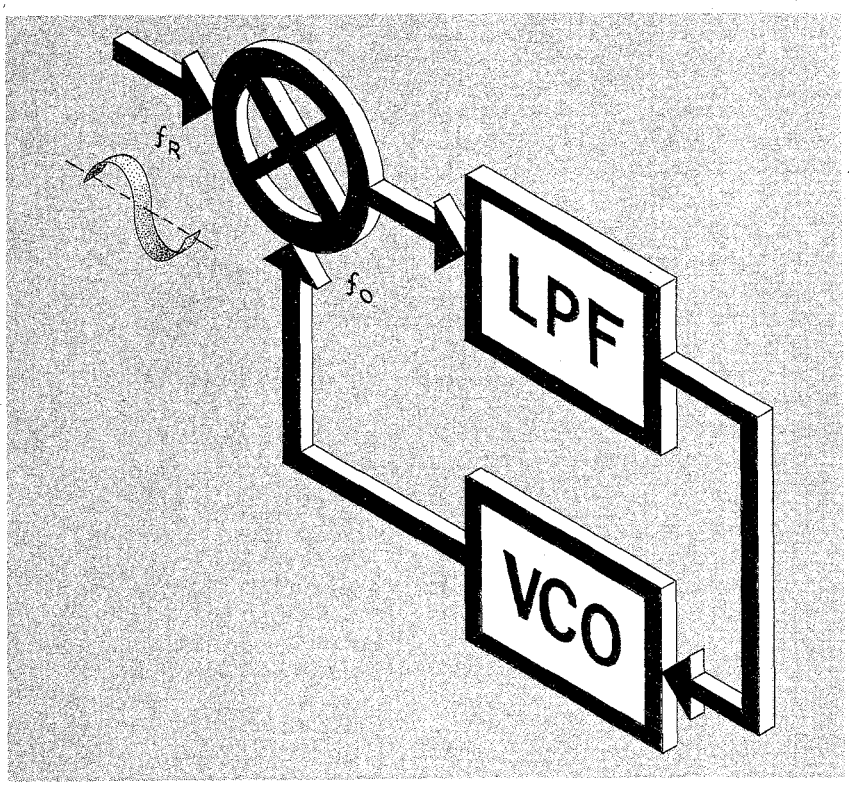
RAY MARSTON



PHASE-LOCKED LOOPS

Learn about phase-locked loops (PLL), and design communications and control circuits with them.

THE PHASE-LOCKED LOOP (PLL) CIRcuit "locks" the frequency and phase of a variable-frequency oscillator to that of an input reference. An electronic servo loop, it provides frequency-selective tuning and filtering without the need for coils or inductors, a desirable feature in miniature, solid-state circuits.

This article examines the theory and basic operating principles of phase-locked loop circuits. It then shows many practical applications for the voltage-controlled oscillator integrated within a monolithic PLL circuit. Subsequent articles in this series will examine communications and control circuits that make use of complete PLL ICs.

Figure 1 is the block diagram of a basic PLL circuit. It consists of blocks representing the phase comparator (sometimes called the phase-detector), low-pass filter (LPF), and a linear, voltage-controlled oscillator (VCO). Prominent applications for PLL ICs include FM demodulators, frequency synthesis, and tone decoding.

PLL principles

The phase comparator receives and compares the phase and frequency of the circuit's output frequency (f_O) with an external input reference frequency (f_R), and generates a corresponding variable output error voltage.

After the error voltage is filtered by the LPF, it is fed to the control input of the VCO so that any frequency or phase differences between f_O and f_R are progressively reduced to zero. When that occurs, the loop is said to be *locked*.

If the VCO's frequency is initially below that of the input reference, the phase comparator's output swings positive. Its filtered voltage output then commands the VCO's frequency to increase until both its frequency and phase precisely match those of the input reference.

Similarly, if the VCO's frequency increases above that of the internal reference, the reverse response takes place. The phase comparator's output decreases, again directing the VCO's frequency to lock to the same frequency as the input reference.

The low-pass filter is the essential part of the PLL circuit that converts the output of the phase detector into a smooth DC control voltage. Because it has a finite time constant, PLL locking is not instantaneous, and the output frequency locks to the *mean* value of f_R, rather than to its instantaneous value. This characteristic is valued for producing clean output frequencies from a noisy input reference frequencies.

Frequency multiplication

In the basic PLL block diagram in Fig. 1, the output signal frequency locks to the mean value of the input frequency so that the input and output frequencies are identical. Figure 2 shows a variation of that circuit in which the output frequency is precisely ten times greater than the input frequency. As a result, the circuit acts like a frequency multiplier.

In the block diagram of Fig. 2, a divide-by-ten counter is inserted in the feedback loop between the VCO output and the input of the phase comparator. Consequently, the phase comparator locks to the output fre-

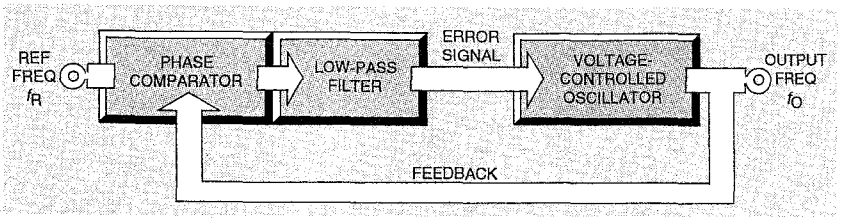


FIG. 1—PHASE-LOCKED LOOP (PLL) circuit.

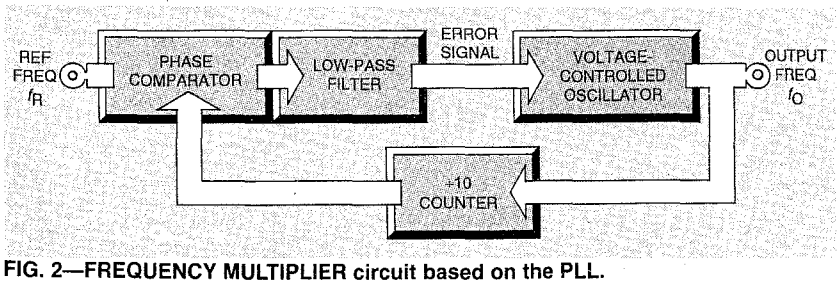


FIG. 2—FREQUENCY MULTIPLIER circuit based on the PLL.

quency of the divide-by-ten counter instead of the output frequency of the VCO.

Therefore, at the lock condition, the VCO's frequency (f_O) is ten times greater than the input reference signal (f_R), and the circuit acts as a 10× frequency multiplier. This circuit can multiply by any number other than ten if it has a counter with an appropriate division ratio in its feedback loop.

Frequency synthesis.

The PLL circuit can also function as a precise programmable frequency synthesizer (see Fig. 3). The reference input frequency of the phase comparator is a fixed precision 1-kHz signal derived from a 1-MHz crystal oscillator through a divide-by-1000 counter.

As in the frequency multiplier circuit, there is a counter in the feedback loop between the VCO's output and the phase comparator's input. However, this circuit is externally programmable, so it can provide any whole-number division ratio between 100× and 1000×.

This feature permits the circuit to generate or synthesize accurate, stable frequencies between 100 kHz and 1 MHz in 1-kHz steps. The VCO circuit in Fig. 3 must have a frequency span range of at least 10 to 1 to cover the required range. Moreover, the frequency step value corresponds to the 1-kHz external input frequency.

High-frequency synthesis

The programmable counter is an essential function of all frequency synthesizers. Practical counters typically respond to maximum input frequencies of only a few megahertz. As a result, the Fig. 3 circuit cannot directly synthesize frequencies higher than a few megahertz. Figures 4 to 6 show three alternative versions of high-frequency PLL synthesizer circuits.

The circuit in Fig. 4 depends on a prescaling technique. An additional *divide-by-X*, fixed-value, high-frequency counter stage (the prescaler) is located between the VCO output and the input of the programmable counter.

This configuration permits the VCO to operate at a frequency X-times higher than the programmable counter stage. In the example shown, the prescaler has a divide-by value of 20×, giving the synthesizer the ability to cover 2 to 20 MHz in 900 discrete steps. A disadvantage is that it causes the step value of the synthesizer to increase by a ratio equal to the prescaler value (i.e., to $20 \times f_R$)—20 kHz in this circuit.

In the Fig. 5 circuit, a mixer technique synthesizes frequencies between 100 and 101 MHz in 1000 discrete steps of 1 kHz. The VCO's output is mixed with a crystal-derived 99.9-MHz frequency before being sent through a low-pass filter to produce a 100-KHz to 1.1-MHz *difference* frequency. That difference frequency then enters the PLL and passes through the programmable counter stages. This scheme permits the VCO frequency to be varied in steps equal to the f_R value, but it limits the VCO's useful span to a few megahertz.

Figure 6 shows how the mixer and prescaler circuits in Fig. 5 can be combined to make a wide-range, high-frequency synthesizer that can generate frequencies between 100 and 120 MHz in 1000 discrete 20-Hz steps. The VCO's output frequency is mixed with a crystal-derived 98-MHz frequency and put through a low-pass filter to produce an output from 2 to 22 MHz.

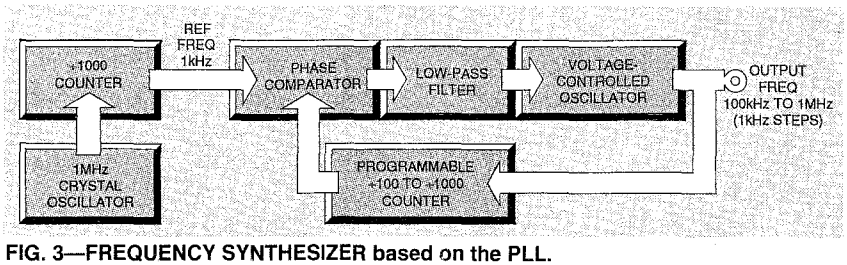


FIG. 3—FREQUENCY SYNTHESIZER based on the PLL.

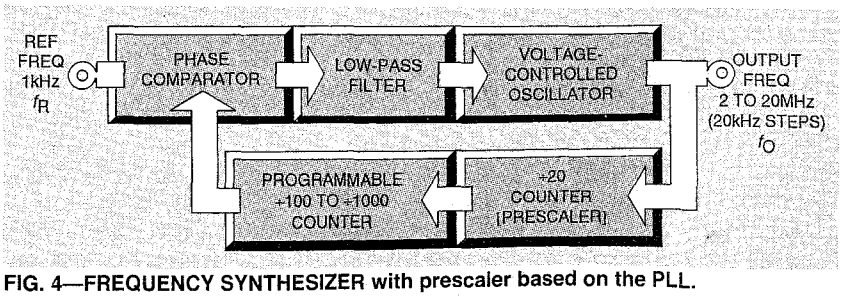


FIG. 4—FREQUENCY SYNTHESIZER with prescaler based on the PLL.

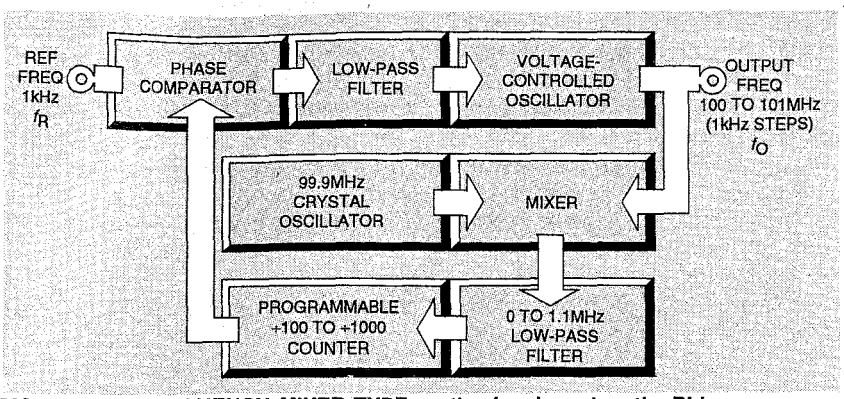


FIG. 5—HIGH-FREQUENCY, MIXER-TYPE synthesizer based on the PLL.

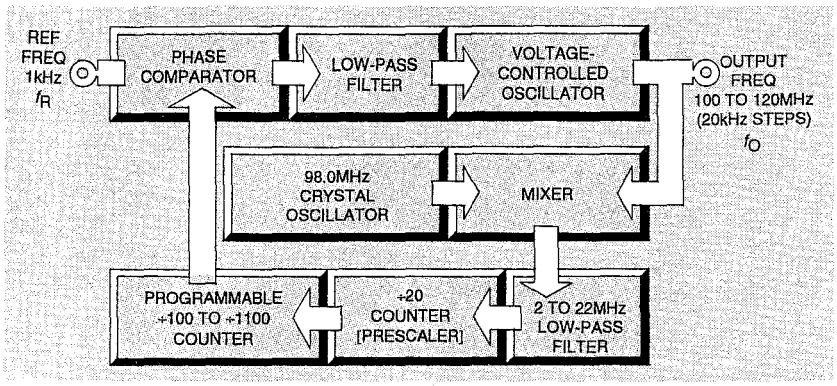


FIG. 6—WIDE-RANGE, HIGH-FREQUENCY synthesizer based on the PLL.

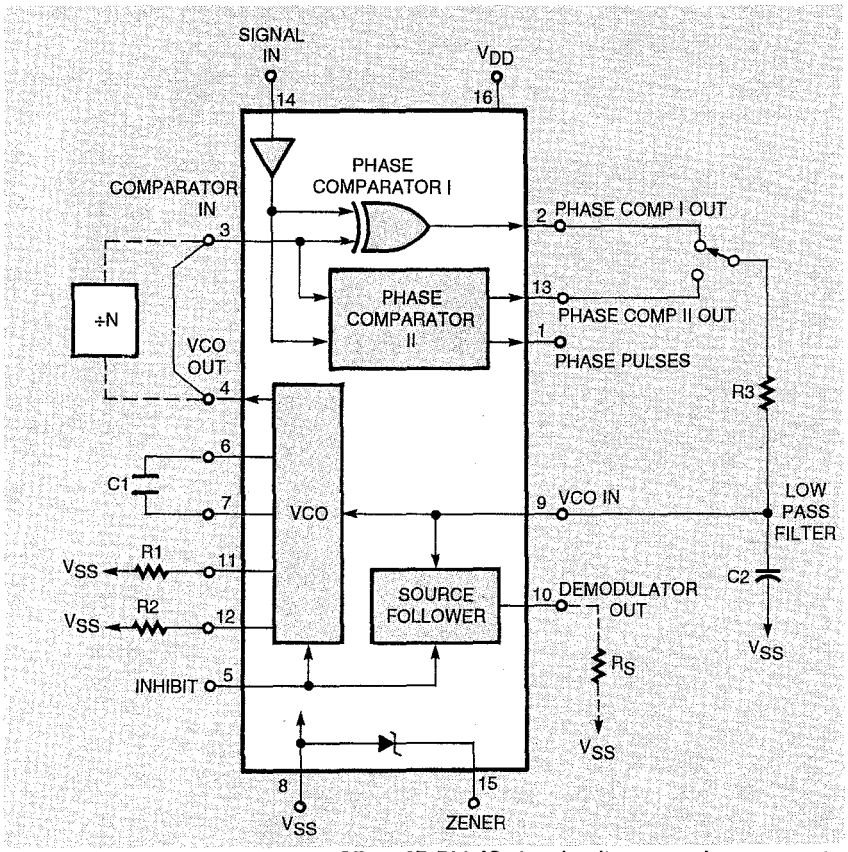


FIG. 7—BLOCK DIAGRAM for the CD4046B PLL IC showing its external components and connections.

That output is then reduced to the 100-kHz to 1.1-MHz range by a divide-by-20 prescaler stage before it is fed back into the PLL through the programmable counter. This synthesizer circuit gives excellent results.

VCO operation.

The voltage-controlled oscillator in high-frequency PLL synthesizers typically must cover a very limited span range. This function is typically performed by a variable capacitor-controlled transistor oscillator with a buffer circuit. By contrast, the VCO in low-frequency synthesizers typically must cover a very wide span range. That circuit is typically a special monolithic CMOS or bipolar IC oscillator.

Some monolithic PLL integrated circuits contain excellent wide-range VCOs that can be used by themselves in practical circuits. An example is the popular Harris CMOS CD4046B, widely alternate-sourced by many other manufacturers including Motorola, National Semiconductor, Philips, and SGS-Thomson. It is also made with HC and HCT CMOS technologies.

The CD4046B PLL IC.

Figure 7 is the block diagram for the CD4046B that includes external components. It consists of a low-power, linear, voltage-controlled oscillator (VCO), a source-follower, a Zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier for a small voltage signal

Phase comparator I, an exclusive OR gate, provides a digital error signal (PHASE COMP I OUT) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it can lock onto the signal input frequencies that are close to harmonics of the VCO's center frequency. It offers good noise-rejection performance, but must be driven by square waves on both pins 3 and 14. It has only a narrow capture-frequency range.

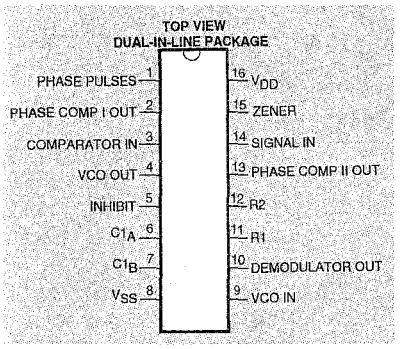


FIG. 8—PINPOUT DIAGRAM for the CD4046B PLL IC in a 16-pin dual-in-line package.

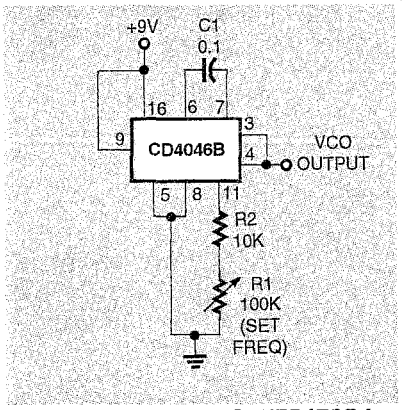


FIG. 9—SQUAREWAVE GENERATOR for 200 Hz to 2 kHz.

Phase comparator II, an edge-triggered digital memory network, provides a digital error signal (PHASE COMP II OUT) and lock-in signal (phase pulses) to indicate a locked condition. It maintains a 0° phase shift between the signal and comparator inputs. It can be driven by crude, non-symmetrical waveforms on pins 3 and 14. Although it has a very wide capture-frequency range, it has poor noise rejection.

The VCO produces an output signal (VCO OUT) whose frequency is determined by the voltage at pin 9 (VCO IN) and the input and the capacitor between pins 6 and 7 ($C1_A$ and $C1_B$, respectively) and resistors R1 and R2 at pins 11 and 12 (R1 and R2, respectively). Resistor R2 permits the minimum operating frequency to be preset. The VCO generates a symmetrical squarewave output that appears on pin 4 (VCO OUT).

The source-follower output of the VCO IN (DEMODULATOR OUT) is used with an external resistor whose value is 10 kilohms or more. When high, the INHIBIT input disables the VCO and source-follower to minimize standby power consumption. The Zener diode between pin 8 (V_{SS}) and 15 (ZENER) has a nominal operating value of 5.6 volts; it can provide supply regulation, if required.

Pin 9 has a nearly infinite input impedance. It can be driven from a high-impedance source. The internal source-follower stage permits the voltage at pin 9 to be externally monitored without loading the source. Pin 5 (INHIBIT) is normally connected to pin 8 to enable both the VCO and the source-follower.

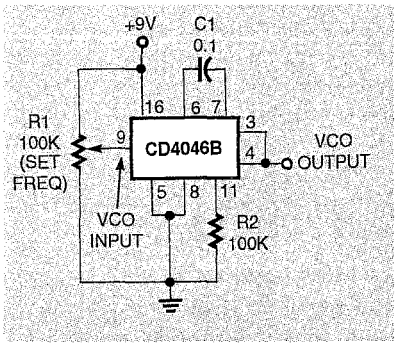


FIG. 10—WIDE-RANGE VCO, variable from near-zero to 1.4 kHz by adjusting the voltage on pin 9.

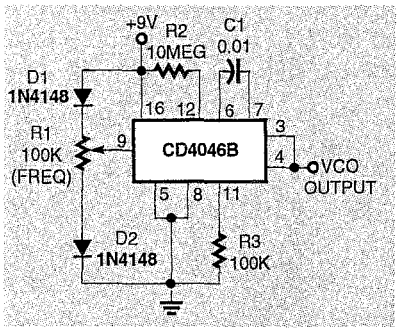


FIG. 11—WIDE-RANGE VCO fully variable down to zero frequency

Figure 8 is the pinout diagram for the CD4046B in a 16-pin dual-in-line package. It will operate over a supply voltage range (V_{DD}) of 3 to 18 volts. Typical power consumption is 70 microwatts, and its VCO frequency is typically 1.3 MHz. The CD4046B has a maximum operating frequency of about 1.6 MHz.

VCO applications

Figures 9 to 17 show various ways to make practical use of the voltage-controlled oscillator section of the CD4046B. In Fig. 9, pin 9 is permanently connected to the supply so that the circuit acts as a basic squarewave oscillator. Its frequency is variable over a 10 to 1 range by adjusting trimmer potentiometer R1.

Pin 4 is tied directly to pin 3 (COMPARATOR IN). If pin 3 is allowed to float, the comparators self-oscillate at about 20 MHz, and superimpose a high-frequency on the VCO output waveform.

Figure 10 shows how to connect the CD4046B as a wide-range VCO. Resistor R2 and capacitor C1 set the maximum frequency that can be obtained, and trimmer potentiometer R1 controls the frequency through the pin 9 voltage. The frequency falls nearly to zero (at a rate of a few cycles per minute) when pin 9 is set at zero volts.

The effective control range of pin 9 varies from about 1 volt above zero to 1 volt below the positive supply value (e.g., po-

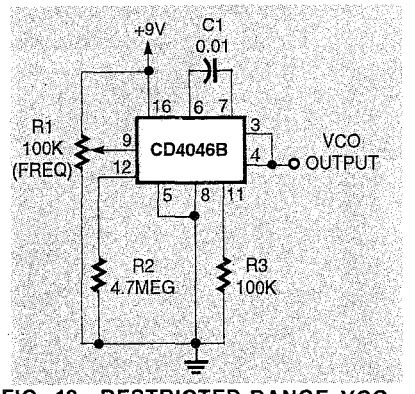


FIG. 12—RESTRICTED-RANGE VCO, variable from 60 Hz to 1.4 kHz with trimmer potentiometer R1.

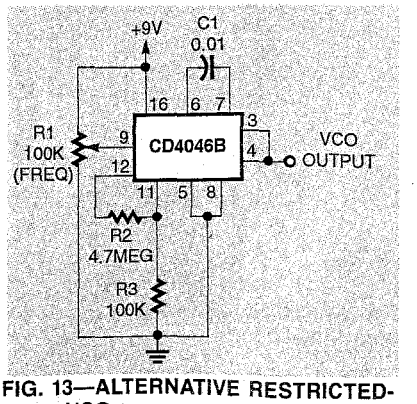


FIG. 13—ALTERNATIVE RESTRICTED-range VCO.

tentiometer R1 has a "dead" control region of several hundred millivolts at either end of its span.)

Figure 11 shows how the "dead" regions of R1 can be eliminated by placing a silicon diode in series with each end of R1 (D1 and D2). The circuit also shows how the minimum operating frequency can be reduced to zero by connecting 10-megohm resistor R2 from pin 12 to pin 16 (V_{DD}). When the frequency is reduced to zero, the VCO output randomly settles to either the logic-0 or logic-1 state.

Figure 12 shows how the resistor at pin 12 can also be connected to pin 8 to set the minimum operating frequency of a restricted-range VCO. The minimum frequency is determined by the combination of R2 and C1, and the maximum frequency is determined by C1 and the parallel value of R2 and R3. Potentiometer R1 can vary the frequency range from 60 Hz to 1.4 kHz.

Figure 13 shows an alternative version of the restricted-range VCO. Its maximum frequency is controlled by R2 and C1, and the minimum frequency is controlled by C1 and R2 and R3. With a suitable choice of values for R2 and R3, the restricted-range VCO can span any range from 1 to 1 to near infinity.

The VCO can be set up to generate a pair of squarewave outputs 180° out-of-phase by connecting the VCO output to the phase comparator input, making pin 14 (SIGNAL IN) high, and taking the 180° out-of-phase output from pin 2, as shown in Figure 14. This circuit takes advantage of the integrated circuit's built-in exclusive OR gate at pin 2.

As shown in Fig. 15, the VCO section of the CD4046B can be disabled by connecting pin 5 high to logic 1. This feature permits the VCO to be gated on and off by external signals. The VCO can be manually gated with pushbutton switch S1 that is connected between pin 5 and ground.

Figure 16 shows how the VCO can be gated electronically by an external inverter stage, one-fourth of a CD4011B, a CMOS NAND gate. Alternatively, if you do not need two-phase ouput capability, Fig. 17 shows how the internal exclusive OR phase detector can control the gate. In this circuit, pin 4 is not connected to pin 3. Ω

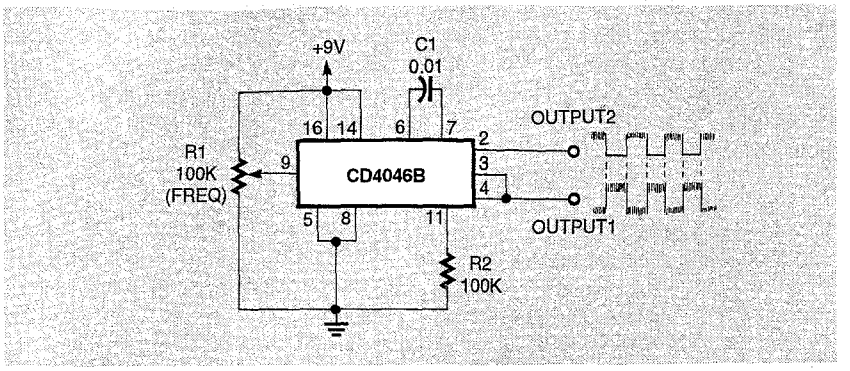


FIG. 14—A TWO-PHASE, WIDE-RANGE VCO.

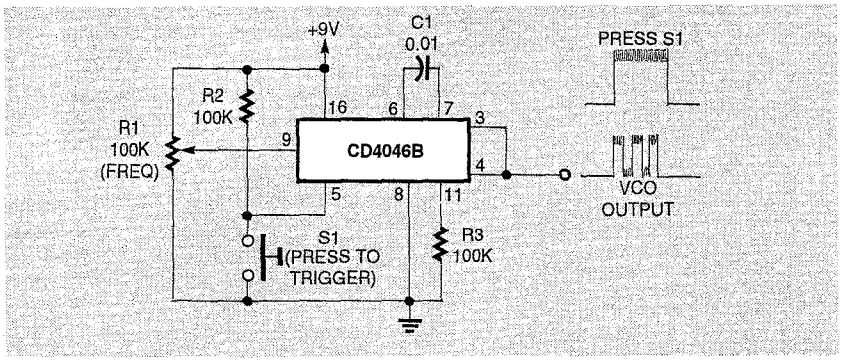


FIG. 15—MANUALLY GATED wide-range VCO.

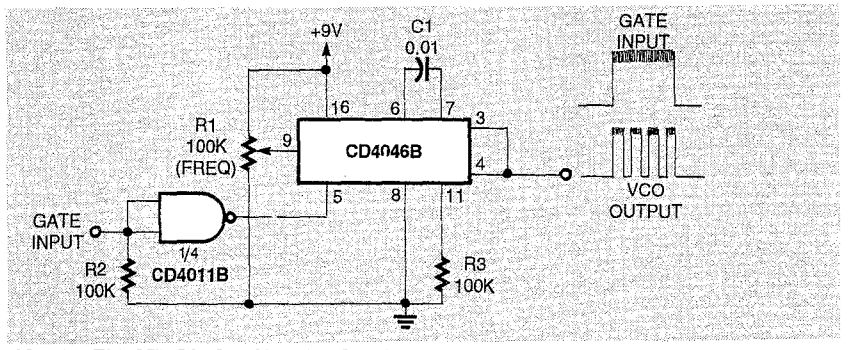


FIG. 16—ELECTRONICALLY GATED, wide-range VCO with an external gate inverter.

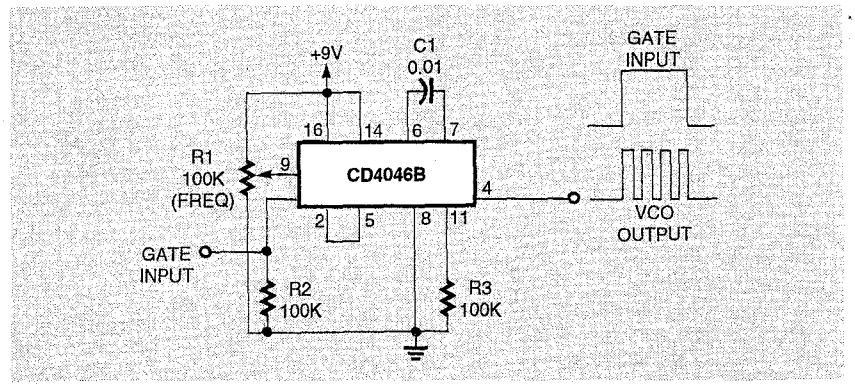


FIG. 17—ELECTRONICALLY GATED, wide-range VCO with an internal exclusive OR phase detector to permit gate inversion.