CMOS CLOCK CIRCUITS

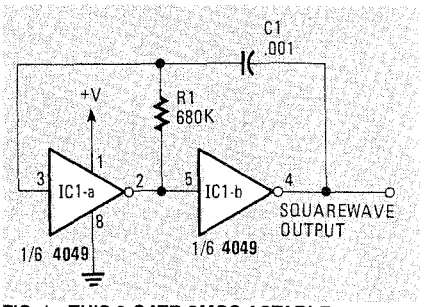

FIG. 1—THIS 2-GATE CMOS ASTABLE operates at 1 kHz with the component values shown.

The next time you need a clock generator, pick out one of these CMOS-based designs.

RAY MARSTON

IN THE SEPTEMBER ISSUE, WE TOOK A look at squarewave-generator circuits. This month, we'll take another look. However, instead of using transistors, op-amps and 555 timer IC's, we'll deal only with designs based on CMOS IC's.

CMOS logic IC's can easily be used to make squarewave-generator or "clock" circuits that are both inexpensive and highly versatile. The outputs can be symmetrical or non-symmetrical, and the oscillators can be either free-running or gated. The gated oscillators can be designed to turn on with either logic-0 or logic-1 signals, and to give either a logic-0 or a logic-1 output when in the "off" mode. You can even use those "cheapo" circuits as simple VCO's (*V*oltage-*C*ontrolled *O*scillators) or as frequency-modulated oscillators.

If you want VCO operation with excellent linearity and versatility, then you have to be slightly more particular about the IC you use. We'll get to that in just a little while. But first, the basics: 2-gate CMOS squarewave-generator or astable circuits.

Two-gate astable oscillators

The simplest way to make an astable circuit is to wire two CMOS inverter stages in series and use the R-C feedback network shown in Fig. 1. That circuit generates a decent squarewave output and operates at about 1 kHz with the component values shown. The frequency is inversely proportional to the R-C time constant, so it can be raised by lowering the values of either C1 or R1. Capacitor C1 must be a non-polarized type; it can have any value from a few tens of pF to several μF. Resistor R1 can have any value from about 47 kilohms to 22 megohms. With those ranges of values, the operating frequency can vary from below 1 Hz to about 1 MHz. For variable-frequency operation, R1 should be replaced by a series combination of a fixed and a variable resistor.

The output of the astable circuit in Fig. 1 switches (when lightly loaded) almost fully between the zero and positive supply rail values. But the R1-C1 junction is prevented from swinging below zero or above the positive rail levels by on-chip clamping diodes at the input of IC1-a. That characteristic causes the operating frequency of the circuit to be somewhat dependent on the supply: Typically, the frequency falls by about 0.8% for a 10% rise in supply voltage. If the frequency is normalized with a 10-volt supply, the frequency falls by 4% at 15 volts or rises by 8% at 5 volts.

The operating frequency of the circuit shown in Fig. 1 is also influenced by the individual gates that are used. You can expect the frequency to vary by as much as 10% between individual IC's. The output symmetry of the waveform also depends on the particular IC used and, in most cases, the circuit will give a non-symmetrical output. In most "hobby" or other non-precision applications, those defects of the basic astable circuit are of little practical importance.

We should note here that for the circuit in Fig. 1—and all of the others that we'll present this month—the supply voltage indicated by "+V" can be anywhere from 3 to 18 volts DC. Also, the CMOS IC's used are all of the "B-series" type (with improved gate-oxide protection.)

Figure 2 shows an improved, "compensated" astable circuit in which R2 is wired in series with the input of IC1-a. That resistor must have a value that is large relative to R1; its main purpose is to allow

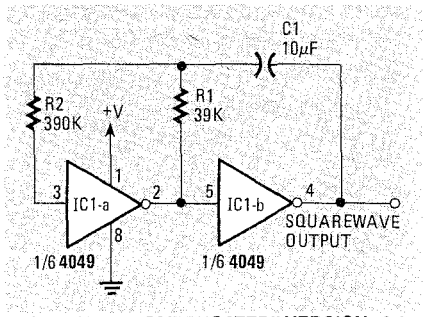

FIG. 2—THE "COMPENSATED" VERSION of the 2-gate astable oscillator has excellent frequency stability with variations in supply voltage.

the R1-C1 junction to swing freely below the zero and above the positive supply rail voltages during circuit operation and thus improve the frequency stability of the circuit. Typically, when R2 is ten times the value of R1, the frequency varies by only 0.5% when the supply voltage is varied between 5 and 15 volts. An incidental benefit of R2 is that it gives a slight improvement in the symmetry of the output of the astable.

The basic and compensated astable circuits of Figs. 1 and 2 can be built with a good number of detail variations, as shown in Figs. 3 to 5. In the basic astable circuit, for example, C1 alternately charges and discharges via R1 and thus has a fixed symmetry. Figures 3 to 5 show how the basic circuit can be modified to give alternate charge and discharge paths for C1 and thus to allow the symmetry to be varied at will.

The circuit in Fig. 3 is useful if you need a highly non-symmetrical waveform (such as a pulse). Capacitor C1 charges in one direction via R2 in parallel with R1, to generate the *mark* (or pulse) part of the waveform. It charges in the reverse direc-

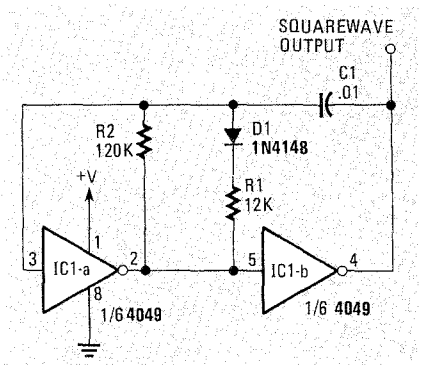

FIG. 3—YOU CAN MODIFY THE 2-gate astable to give a non-symmetrical output. The "mark" time is controlled by the parallel combination of R1 and R2. The "space" time is controlled by only R2.

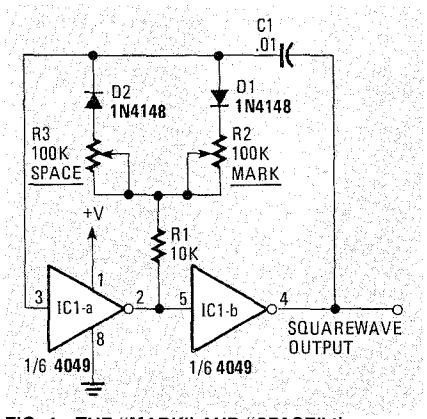

FIG. 4—THE "MARK" AND "SPACE" times can be independently varied by R2 and R3 respectively.

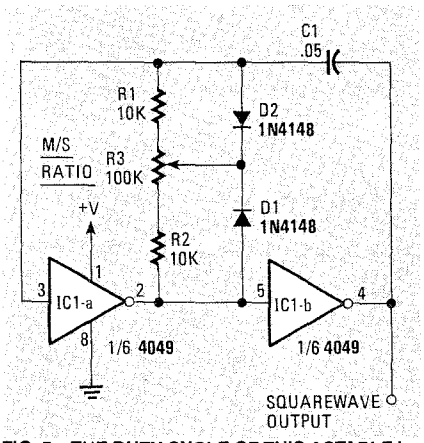

FIG. 5—THE DUTY CYCLE OF THIS ASTABLE is fully variable from 1:11 to 11:1.

tion via R2 only, to give the *space* between the pulses.

Figure 4 shows the modifications for generating a waveform with independently variable mark and space times; the mark time is controlled by R1, R2, and D1, and the space time is controlled by R1, R3, and D2.

Figure 5 shows the modifications to give a variable duty-cycle (or mark/space ratio) output while maintaining a near-constant frequency. Here, C1 charges in one direction via D2 and the lower half of R3 and R2, and in the other direction via D1 and the upper half of R3 and R1. The duty cycle can be varied over a range of 1:11 to 11:1 via R3.

Figure 6 shows a couple of ways of using the basic astable circuit as a very simple VCO. The circuit in Fig. 6-a can be used to vary the operating frequency over a limited range via an external voltage. For satisfactory operation, R2 must be at least twice as large as R1. Its actual value depends on the required frequency-shift range: A low R2 value gives a large frequency-shift range, and a larger R2 value gives a small frequency-shift range. The circuit in Fig. 6-b acts as a special-effects VCO in which the oscillator frequency rises with input voltage, but switches off completely when the input voltage falls below a value preset by R3.

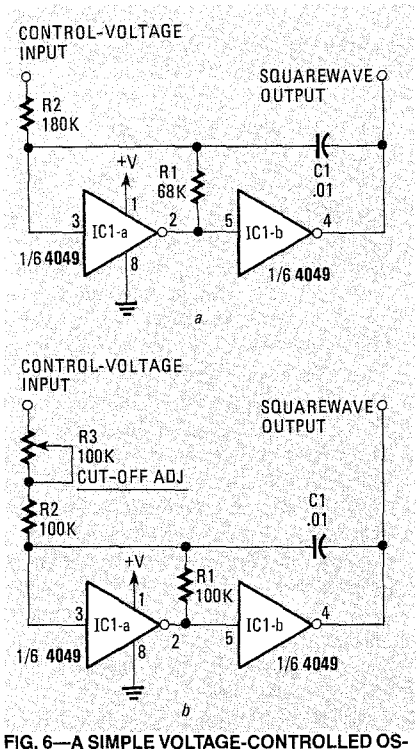

FIG. 6—A SIMPLE VOLTAGE-CONTROLLED OSCILLATOR or VCO is shown in *a*. Shown in *b* is a VCO that cuts off when V_{IN} falls below a value that is preset by R3.

Gated astable circuits

All of the astable circuits of Figs. 1 to 6 can be made using NAND or NOR gates instead of inverters. Simply replace the inverters with one of the gates as shown in Fig. 7.

Using NAND and NOR gates instead of inverters has a practical advantage—it lets you modify all of the circuits in Figs. 1–6 for gated operation. In other words, the astables can be turned on and off by external signals. All you have to do is to use a 2-input NAND (4011B) or NOR (4001B) gate in place of the inverter in the IC1-a position, and apply a control signal to one of the gate input terminals. By choosing the appropriate gate, you can control your astable by either a high or a low gate signal. That is shown by the two basic versions of the gated astable multivibrator in Figs. 8 and 9.

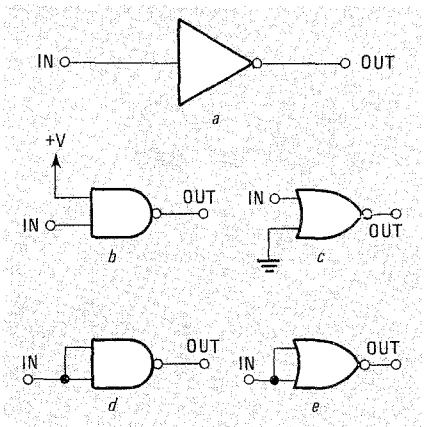

FIG. 7— TWO-INPUT NAND OR NOR gates can be used as inverters. As we'll see, they permit gated operation. As with any other CMOS IC, be sure to tie all unused inputs to one of the supply rails.

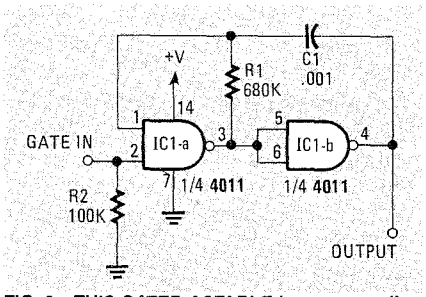

FIG. 8—THIS GATED ASTABLE has a normally-low output. It is gated on by a high input.

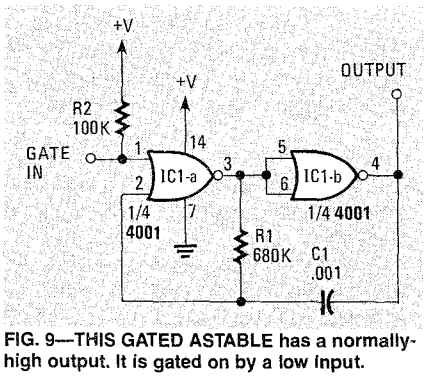

FIG. 9—THIS GATED ASTABLE has a normally-high output. It is gated on by a low input.

Note specifically from those two circuits that the NAND version is gated on by a logic-1 input and has a normally-low output, while the NOR version is gated on by a logic-0 input and has a normally high output. Pull-up (or pull-down) resistor R2 can be eliminated from the circuits if IC1-a is direct-coupled from the output of a preceding CMOS logic stage.

In the basic gated astable circuits of Figs. 8 and 9, the output signal terminates as soon as the gate drive signal is removed. Consequently, any noise present at the gate terminal also appears at the outputs of those circuits. Figures 10 and 11 show how to modify the circuits to over-

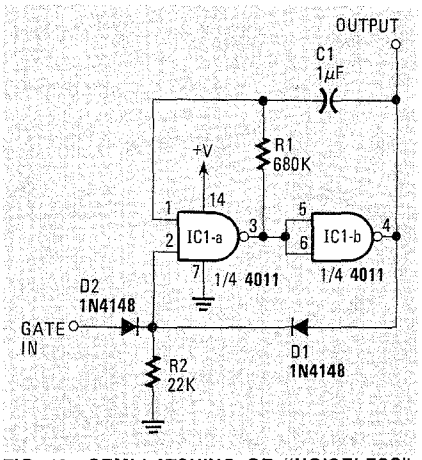

FIG. 10—SEMI-LATCHING OR "NOISELESS" gated astable has a normally-low output and is gated on by a high input.

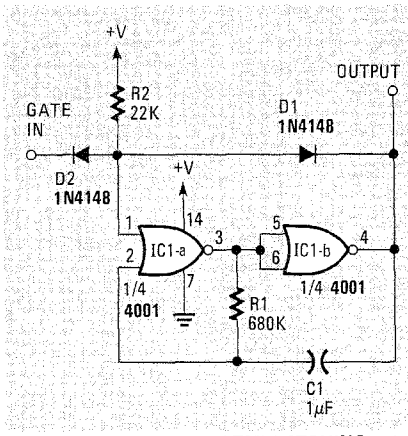

FIG. 11—ALTERNATIVE SEMI-LATCHING astable has a normally-high output and is gated on by a low input.

come that problem. There, the gate signal of IC1-a is derived from both the "outside world" and from the output of IC1-b via the diode OR gate (D1, D2, and R2). As soon as the circuit is gated from an external signal applied via D2, the output of IC1-b reinforces or self-latches the gating via D1 for the duration of one-half astable cycle. That eliminates any effects of a noisy external gate signal. The outputs of the "semi-latching" gated astable circuits are thus always complete numbers of half cycles.

Ring-of-three circuits

The 2-gate astable circuit is not generally suitable for direct use as a "clock" generator with fast-acting counting and dividing circuits. That's because it tends to pick up and amplify any supply-line noise during the "transitioning" parts of its operating cycle and to thus produce squarewaves with "glitchy" leading and trailing edges. A far better type of clock generator circuit is the *ring-of-three* astable that is shown in Fig. 12.

The Fig. 12 ring-of-three circuit is similar to the basic 2-gate astable, except that its "input" stage (IC1-a–IC1-b) acts as an ultra-high-gain non-inverting amplifier and its main timing components (R1-C1) are transposed (relative to the 2-gate astable). Because of the very high overall gain of the circuit, it produces an excellent and glitch-free squarewave output, ideal for clock-generator use.

The basic ring-of-three astable can be subjected to all the design modifications that we've already looked at for the basic

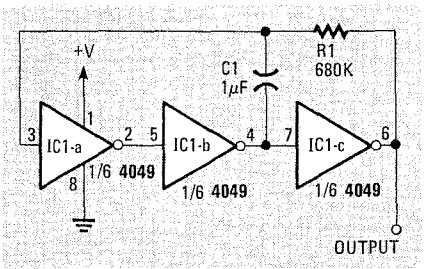

FIG. 12—THE "RING-OF-THREE" astable makes an excellent clock generator.

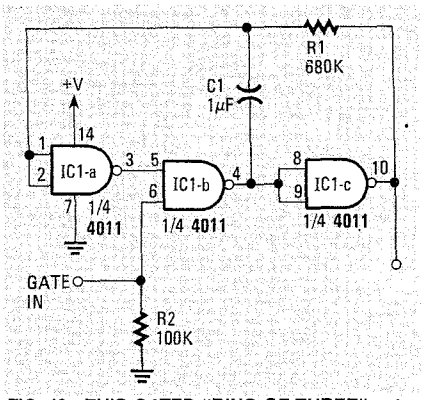

FIG. 13—THIS GATED "RING-OF-THREE" astable has a normally-low output and is gated on by a logic-1 signal.

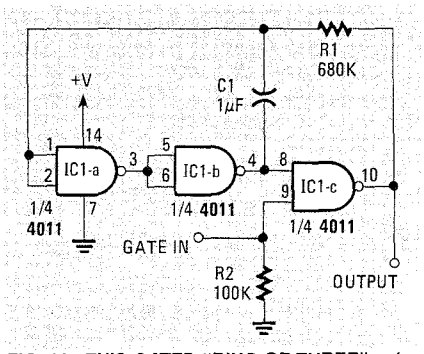

FIG. 14—THIS GATED "RING-OF-THREE" astable has a normally-high output and is gated on by a logic-1 signal.

2-gate astable—it can be used in either basic or compensated form and can give either a symmetrical or non-symmetrical output, etc. The most interesting variations of the circuit occur, however, when it is used in the gated mode, since it can be gated via either the IC1-b or IC1-c stages. Figures 13 to 16 show four variations on that gating theme.

The circuits in Figs. 13 and 14 are both gated on by a logic-1 input signal, but the

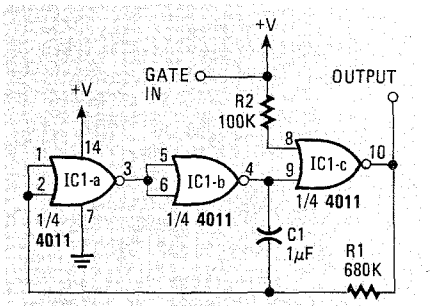

FIG. 15—THIS ASTABLE IS GATED on by a logic-0 signal and has a normally low output.

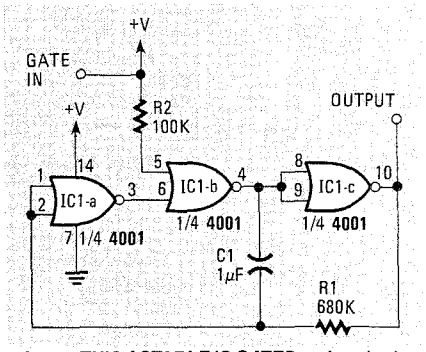

FIG. 16—THIS ASTABLE IS GATED on by a logic-0 signal and has a normally high output.

circuit in Fig. 13 has a normally-low output, while that of Fig. 14 is normally-high. Similarly, the circuits in Fig. 15 and 16 are both gated on by a logic-0 signal, but the output of the circuit in Fig. 15 is normally-low, while that of Fig. 16 is normally-high.

4046 VCO circuits

To close this look at CMOS squarewave generator circuits, let's consider some practical VCO applications of the 4046 phase-locked loop (PLL) IC. Figure 17 shows the internal block diagram and pinout of the 4046, which contains a couple of phase comparators, a VCO, a Zener diode, and a few other bits and pieces.

For our present purpose, the most important part of the chip is the VCO section. That VCO is a highly versatile device: It produces a well-shaped symmetrical squarewave output, has a top-end frequency limit in excess of 1 MHz, has a voltage-to-frequency linearity of about 1%, and can easily be "scanned" through a 1,000,000:1 range by an external voltage applied to the VCO input terminal. The frequency of the oscillator is governed by the value of a capacitor (minimum value 50 pF) connected between pins 6 and 7, by the value of a resistor (minimum value 10K) wired between pin 11 and ground, and by the voltage (any value from zero to the supply voltage) applied to VCO-input pin 9.

Figure 18 shows the simplest possible way of using the 4046 VCO as a voltage-controlled squarewave generator. In that circuit, the C1-R1 combination deter-

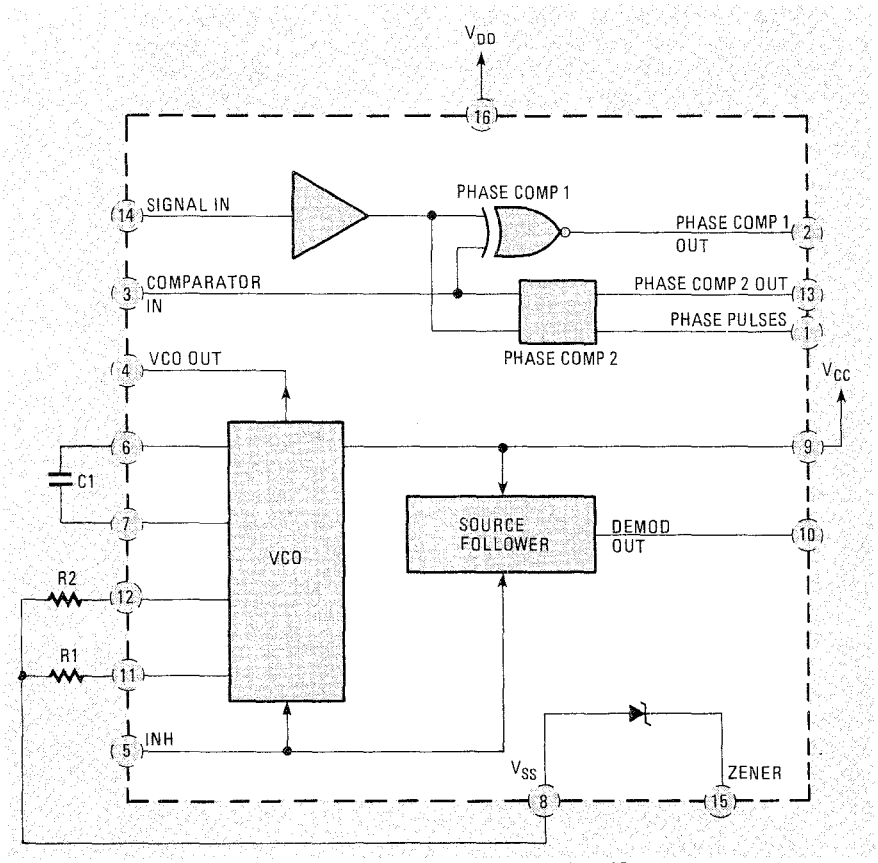

FIG. 17—INTERNAL BLOCK DIAGRAM of the 4046 phase-locked loop IC.

mines the maximum frequency that can be obtained (with the pin 9 voltage at maximum) and R2 controls the actual frequency by applying a control voltage to pin 9:

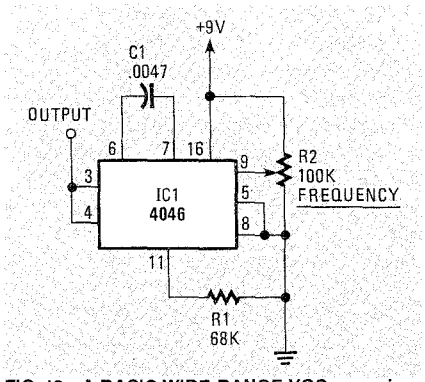

FIG. 18—A BASIC WIDE-RANGE VCO spanning from about zero to about 5 kHz (determined by R2).

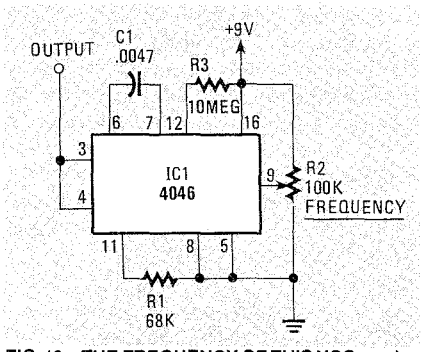

FIG. 19—THE FREQUENCY OF THIS VCO can be varied all the way down to zero.

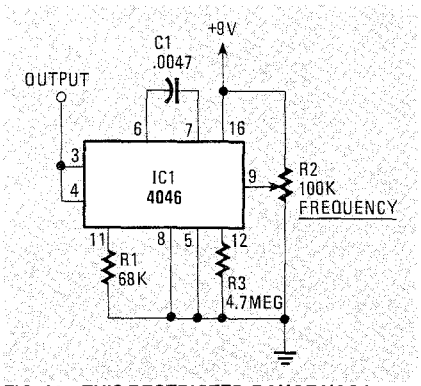

FIG. 20—THIS RESTRICTED-RANGE VCO has a frequency range from about 72 Hz to 5 kHz.

The frequency falls to a very low value (a fraction of a Hz) with pin 9 at zero volts. The effective control-voltage range of pin 9 varies from roughly 1 volt below the supply value to about 1 volt above ground, and gives a frequency span of about 1,000,000:1. Ideally, the supply voltage to the circuit should be regulated.

We've said above that the frequency of the circuit shown in Fig. 18 falls to *near*-zero when the input voltage is reduced to zero. Figure 19 shows how the circuit can be modified so that the frequency falls all the way to zero—all that's needed is a high-value resistor (R3) between pins 12 and 16. Note here that, when the frequency is reduced to zero, the VCO output randomly settles in either a logic 0 or a logic 1 state.

Figure 20 shows how the pin-12 resistor can be used to determine the minimum operating frequency of a restricted-range VCO. In that circuit, f_{MIN} is determined by C1-R2 and f_{MAX} is determined by the combination of C1 and the parallel resistance of R1 and R2.

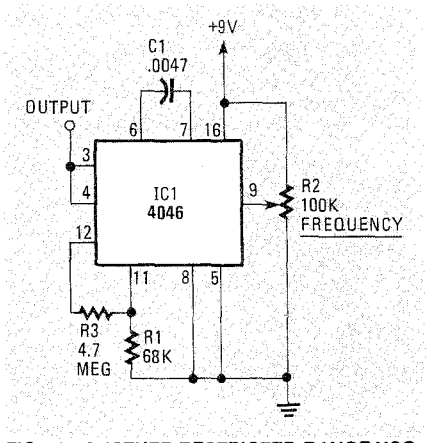

FIG. 21—ANOTHER RESTRICTED-RANGE VCO. The maximum frequency is determined by the C1-R1 time constant; the minumum frequency is determined by the time constant C1(R1 + R3).

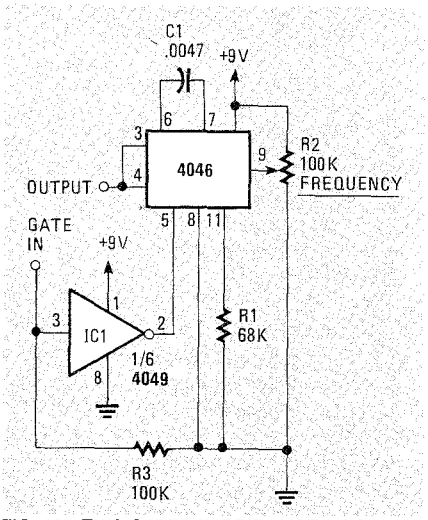

FIG. 22—THIS GATED WIDE-RANGE VCO uses an external inverter.

Figure 21 shows an alternative version of the restricted-range VCO, in which f_{MAX} is controlled by C1-R1 and f_{MIN} is determined by C1 and the series combination of R1 and R2. Note that, by making a suitable choice of the R1 and R2 values, the circuit can be made to "span" any desired frequency range from 1:1 to near-infinity.

Finally, it should be noted that the VCO section of the 4046B can be disabled by taking pin 5 of the package high (to logic 1 level) or enabled by taking pin 5 low. That feature makes it possible to gate the VCO on and off by external signals. Figure 22 illustrates that feature and shows how the basic voltage-controlled oscillator circuit can be gated via a signal applied to an external inverted stage. **R-E**